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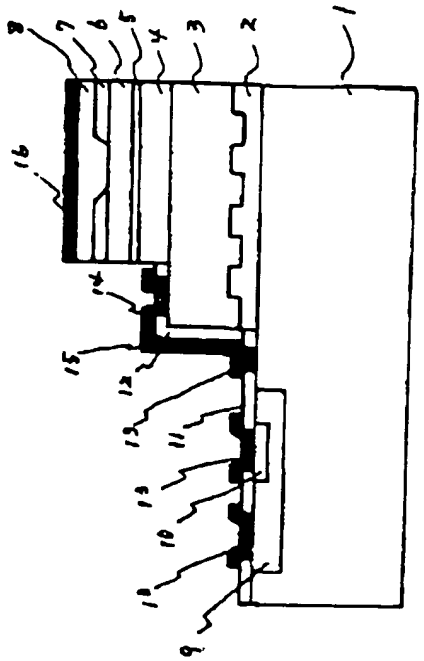
TITLE : SEMICONDUCTOR PHOTOELECTRONIC DEVICE



ABSTRACT : PURPOSE: To integrate a light-emitting element, a light-receiving element and an electronic element on a single substrate and to obtain an photoelectronic device with high utility, by selectively utilizing the upper or lower face of the Si single-crystal substrate and by superposing thereon an amorphous insulation film, a thin film of a compound semiconductor and multilayer thin film of said compound semiconductor.

CONSTITUTION: An SiO_2 film 2 on an N type Si substrate 1 is provided, on the surface thereof, with rectangular stripe grooves with a depth of $10\sim10^{5-}$ and a width of 0.1~10μm by means of etching. Amorphous or polycrystalline N type GaAs 3 is then deposited thereon by the vapor growth, and is heated so that it is rearranged along the grooves and that single crystal is caused to grow. Subsequently, an N type AlGaAs layer 4, an AlGaAS active layer 5, a P type AlGaAs layer 6 and a P type GaAs layer 8 are epitaxially deposited to form a laser diode. An N^+ layer 10 is provided in the P^+ layer 9 of the substrate 1 to form an NPN transistor. These are provided with protective films 11 and 12, electrodes 8, 13 and 14 and wiring 15, respectively. According to this construction, the intensity of laser beams can be controlled with the base current in the transistor. Further, it is also possible to integrate a laser element, a light-receiving element and a driving element on one face while integrating a driving element and a signal processing arithmatical element on the opposite face.

[*Japanese text, sheet 473 (1), bibliographic section*]

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Request for examination: Request has not been made.
Number of inventions: 1
(Total of 6 pages)

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(54) AN OPTOELECTRONIC SEMICONDUCTOR DEVICE

(21) Patent Application No.: S59[1984]-230947
(22) Application Filed: November 1, 1984

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[1] *Here and below, the readings given for Japanese personal names, especially given names, should be considered unconfirmed as there are in general a number of possible readings therefor. —Tr.*

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[*Japanese text, sheet 473 (1), Specification, column —1—*]

SPECIFICATION

1. TITLE OF INVENTION

An Optoelectronic Semiconductor Device

2. CLAIMS

(1) An optoelectronic semiconductor device characterized in that it comprises a monocrystalline silicon substrate, an amorphous insulator film present on all or a part of a front or back surface of said monocrystalline silicon substrate, a compound semiconductor thin film present on all or a part of said amorphous insulator film surface, and a multilayer compound semiconductor thin film present on all or a part of said compound semiconductor thin film surface.

(2) An optoelectronic semiconductor device according to claim 1 characterized in that the aforesaid compound semiconductor thin film comprises a monocrystalline thin film formed on the aforesaid amorphous insulator film surface by a method of graphoepitaxial growth, and the aforesaid multilayer compound semiconductor[2] comprises a multilayer monocrystalline thin film formed on the aforesaid compound semiconductor thin film surface by a method of epitaxial growth.

[*Japanese text, sheet 473 (1), Specification, column —2—*]

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[2] *Sic viz absence of* "thin film" *and resulting awkward reference to antecedents. —Tr.*

(3) An optoelectronic semiconductor device according to claim 1 characterized in that at least one of the aforesaid monocrystalline silicon substrate, the aforesaid compound semiconductor thin film, or the aforesaid multilayer compound semiconductor thin film is employed as a constituent material of a photoemissive element possessing electronic-optical conversion capability or a photoreceptive element possessing optical-electronic conversion capability.

(4) An optoelectronic semiconductor device according to claim 1 or claim 3 characterized in that at least one of a plurality of electronic elements possessing signal processing and operational [logic] capabilities or an electronic element capable of causing operation of the aforesaid photoreceptive element or the aforesaid photoemissive element comprising silicon semiconductor is formed on a front or back surface of the aforesaid monocrystalline silicon substrate.

3. DETAILED DESCRIPTION OF THE INVENTION

Industrial Field of Use

The present invention relates to substrate structure and function in an optoelectronic semiconductor device.

Conventional Art

Optical techniques are beginning to be introduced to replace electronic [*Japanese text, sheet 474 (2), Specification, column —3—*] techniques in information transmission and information processing in order to take advantage of the high speed, multiplexing ability,

precision, and so forth which are characteristic of light. Typical examples of this are audio and image reproduction techniques combining optical disks and semiconductor lasers, long-distance optical communication techniques employing laser light and optical fibers, for example, and so forth. In such optical systems, photoemissive elements which emit laser light or the like, photoreceptive elements which convert transmitted optical signals into electrical signals, and electronic devices which drive such photoemissive/photoreceptive elements can be said to constitute the heart of the optical system.[3] Such optical elements and electronic devices are beginning to be integrated for the purpose of increasing system miniaturization, performance, speed, and so forth. That is, semiconductor lasers (LDs), photodiodes (PDs), and field effect transistors (FETs) are being fabricated on the same semiconductor substrate surface, with the LDs and PDs being driven by the FETs. For example, as [described] at 1984 Institute of Telecommunications Engineers Collected Lectures 4-28, Lecture No. 974,[4] an indium phosphide FET and an LD comprising an indium/gallium/arsenic/phosphorous system compound semiconductor have been fabricated on indium phosphide compound semiconductor substrate, with laser light being modulated by the FET. Furthermore, as [described] at Same Collected [Lectures] 4-24, [*Japanese text, sheet 474 (2), Specification, column —4—*] Lecture No. 970, a photodiode and an FET have been fabricated on the same substrate surface. Conventionally, indium phosphide (InP) substrate and gallium arsenic (GaAs) substrate have primarily been employed as the semiconductor substrate used in such optoelectronic semiconductor devices. Fabrication of semiconductor laser elements having good characteristics is easy on such substrates.

In addition, there are also instances in which a compound semiconductor has been grown on silicon substrate to fabricate an optoelectronic semiconductor device. At 1984 Institute of

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[3] *Here and below, somewhat circular and repetitive style reflects same in Japanese text. —Tr.*

[4] "1984 Dentsu Gakkai Kouen Ronbunshu 4-28, Kouen Bangou 974" *in the Japanese text. Similar comment applies to references below. —Tr.*

Telecommunications Engineers Collected Lectures 2-17, Lecture No. 255, germanium was epitaxially grown on monocrystalline silicon substrate, with gallium arsenide being furthermore epitaxially grown on the surface thereof, and an FET being fabricated on that gallium arsenide. At [t]he 16th Conference on Solid State Devices and Materials 1984, Lecture No. C 11, just as in the aforementioned example, crystalline gallium arsenide was grown on monocrystalline silicon substrate with germanium intervening therebetween, following which a laser diode was fabricated on the surface thereof and [the device] was made to produce pulsed emission.

[*Japanese text, sheet 474 (2), Specification, column —5—*]

Problems to Be Solved by Invention

However, the conventional art described above has problems such as the following. To wit, besides problems affecting characteristics such as the fact that drive voltage cannot be made [very] high for FETs and other such electronic devices on compound semiconductor substrates, the fact that there are a large number of states at the MIS (Metal-Insulator-Semiconductor) interface and it is difficult to control threshold voltage, the fact that mobility of holes is low, and the fact that the forbidden band is too wide, there are also the problems of poor stability and reliability. Furthermore, the compound semiconductor substrate itself also suffers from such problems as poor crystallinity, high substrate cost, tendency to fracture, and unsuitability for large diameters. Accordingly, an optoelectronic semiconductor device employing conventional compound semiconductor substrate and having sufficiently satisfactory characteristics when used in practical applications has not been obtained.

With regard to [devices] employing monocrystalline silicon substrate, because there is a difference of 4% or more in the lattice constant[5] of monocrystalline silicon and monocrystalline gallium arsenide, lattice mismatch occurs therebetween. For this reason, lattice defects and lattice strain being produced in monocrystalline gallium arsenide, there has been the problem that it has not been possible to obtain an electronic element or optical element having good characteristics on monocrystalline gallium arsenide, [*Japanese text, sheet 474 (2), Specification, column —6—*], and [such elements] are lacking in reliability and reproducibility.

Solution of such problems is therefore a purpose of the present invention, and as such its object is to provide a highly practical optoelectronic semiconductor device wherein electronic element(s), photoreceptive element(s), and photoemissive element(s) having excellent characteristics and high reliability are integrated on the same substrate.

Means for Solving Problems

The optoelectronic semiconductor device of the present invention is characterized in that it comprises a monocrystalline silicon substrate, an amorphous insulator film present on all or a part of a front or back surface of said monocrystalline silicon substrate, a compound semiconductor thin film present on all or a part of said amorphous insulator film surface, and a multilayer compound semiconductor thin film present on all or a part of said compound semiconductor thin film surface; the aforesaid compound semiconductor thin film comprising a monocrystalline thin film formed by a method of graphoepitaxial growth; the aforesaid multilayer compound semiconductor thin film comprising a multilayer monocrystalline thin film formed by a method of epitaxial growth; the aforesaid monocrystalline silicon substrate, the aforesaid compound semiconductor thin film, and the aforesaid multilayer compound

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[5] *There appears to be a minor typographical error in the Japanese text at this location. —Tr.*

semiconductor thin film being employed as constituent materials of a photoemissive [*Japanese text, sheet 475 (3), Specification, column —7—*] element or a photoreceptive element; and an electronic circuit possessing signal processing and operational [logic] capabilities and an electronic element capable of causing operation of a photoreceptive element or photoemissive element comprising silicon semiconductor being formed on a front or back surface of the aforesaid monocrystalline silicon substrate.

Working Example 1

A working example of the present invention is shown in FIG. 1. At FIG. 1, 1 is *n*-type monocrystalline silicon substrate having a (100) facial orientation and an impurity concentration on the order of 10^{15} cm^{-3}. 2 is an amorphous insulator film comprising SiO_2 (silicon dioxide) several microns in thickness formed on the aforesaid *n*-type silicon substrate surface by the thermal oxidation method or the chemical vapor phase growth method[6], or the sputtering method, or the like. A rectangular stripe channel having a depth on the order of 10 to 10000 angstroms and a width on the order of 0.1 to 10 microns is formed on the surface of this amorphous insulator film by etching at a pitch of 0.1 to 10 microns. Among the etching methods [which may be used here] are wet etching methods employing hydrogen-fluoride-type etchants and reactive ion etching methods employing Freon (CF_4) or the like as reactive gas. [The dimension in] the long direction of the channel is [*Japanese text, sheet 475 (3), Specification, column —8—*] arbitrary. While the present working example employs SiO_2 as amorphous insulator film, silicon nitride (Si_xN_y), alumina (Al_2O_3), and so forth may also be used. 3 is an *n*-type monocrystalline gallium arsenide thin film which has been graphoepitaxially grown on the aforesaid amorphous insulator film. Graphoepitaxial growth of monocrystalline gallium arsenide [may be carried out

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[6] *Term in Japanese text is different from Japanese term ordinarily used for* "chemical vapor deposition." *Similar comment applies to terms below. —Tr.*

by] first employing the vapor phase growth method, the organometallic vapor phase growth method, the molecular beam epitaxial method, or the like to deposit an amorphous or polycrystalline gallium arsenide thin film on the surface of an SiO_2 film possessing channel(s) as shown at 2, and then heating using a laser, infrared lamp, heater, or the like and causing the gallium arsenide to be reoriented parallel to the channel(s), permitting monocrystalline growth. The graphoepitaxially grown monocrystalline gallium arsenide thin film [may be] several to several tens of microns in thickness. To improve monocrystallinity over the gallium arsenide surface, the liquid phase growth method, vapor phase growth method, or other such thermal equilibrium growth method may be used to grow monocrystalline gallium arsenide of good film quality on the graphoepitaxial gallium arsenide crystal surface. The graphoepitaxial method may be utilized not only with gallium arsenide, but also in the growth of other Group [*illeg.*]-V system compound [*Japanese text, sheet 475 (3), Specification, column —9—*] semiconductors, Group II-VI system compound semiconductors, Group IV compound semiconductors, silicon, and other crystals. At FIG. 1, 4 through 8 are compound semiconductor thin films which together with 3 constitute a double heterostructure *p-n* junction semiconductor laser. 4 is a first cladding layer comprising *n*-type monocrystalline aluminum/gallium/arsenic, 5 is an active layer comprising monocrystalline aluminum/gallium/arsenic of low impurity concentration, 6 is a second cladding layer comprising *p*-type monocrystalline aluminum/gallium/arsenic, 7 is a current confinement layer comprising *n*-type gallium/arsenic, and 8 is a surface cap layer comprising *p*-type gallium/arsenic. While a double heterostructure semiconductor laser diode is fabricated in the present working example, in addition hereto it is also possible to fabricate distributed-feedback-type lasers, multiquantum wells, superlattice lasers, and so forth. 16 is an electrode comprising Au-Zn/Au for making ohmic contact from the *p*-type gallium/arsenic layer of 8.

9 is a p^+-type layer formed by introduction of impurities within the *n*-type monocrystalline silicon substrate, and 10 is an n^+-type layer formed by introduction of

impurities within the aforementioned *p*-type layer. An *npn*-type [*Bridging seal at bottom of column illegible. —Tr.*] [*Japanese text, sheet 475 (3), Specification, column —10—*] bipolar transistor is formed by 1, 9, and 10. That is, 1 is a collector, 9 is a base, and 10 is an emitter. 11 is a silicon substrate surface passivation film, and 12 is a compound semiconductor layer surface protection film. 13 is an Al electrode that makes ohmic contact from the silicon. 14 is an Au-Ge/Au electrode that makes ohmic contact from the *n*-type monocrystalline gallium arsenide thin film. 15 is wiring traces.

In the structure at FIG. 1, the *n* side of the semiconductor laser diode is connected to the collector region of the bipolar transistor. Furthermore, with[7] the *p* side of the semiconductor laser diode at a positive electric potential and the emitter of the bipolar transistor at a negative electric potential, application of a given potential to the base of the bipolar transistor will cause current to flow at the semiconductor laser diode, [producing] laser oscillation, and this optoelectronic semiconductor device will emit laser light. The intensity of the emitted laser light can be controlled by means of the current at the base of the bipolar transistor.

The present working example is an example of an optoelectronic semiconductor device in which a semiconductor laser and a bipolar drive transistor have been [*Bridging seal at bottom of column illegible. —Tr.*] [*Japanese text, sheet 476 (4), Specification, column —11—*] integrated. A field effect transistor, static induction transistor, or the like may be used in place of the bipolar transistor. Furthermore, there is no reason that a plurality of semiconductor lasers or a plurality of transistors cannot be integrated [thereon].

Working Example 2

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[7] *There appears to be a minor typographical error in the Japanese text at this location. —Tr.*

A second working example of the present invention is shown in FIG. 2. This working example is characterized by the fact that a semiconductor laser, a photodiode, and a drive transistor are integrated on the same substrate surface.

At FIG. 2, 17 is a *p*-type monocrystalline silicon substrate. 1' is an *n*-type monocrystalline silicon film which has been epitaxially grown on the aforesaid *p*-type monocrystalline silicon substrate. The specifications and purpose for using the present *n*-type monocrystalline silicon film are identical to those of the *n*-type monocrystalline silicon substrate of 1 described at Working Example 1. 2' through 8' and 16' of FIG. 2 correspond to 2 through 8 and 16 described at Working Example 1. 18 is a P^+-type[8] diffusion layer for isolation of elements. 19, 21, and 23 are P^+-type diffusion layers; 20 and 22 are n^+-type diffusion layers. 24 is a silicon surface passivation film, and 25 through 32 are metal electrodes that make ohmic contact from [*Japanese text, sheet 476 (4), Specification, column —12—*] respective regions of the silicon. 1" is a collector, 19 is a base, and 20 is an emitter, and 25, 26, and 27 are respectively electrodes for the collector, base, and emitter, forming a first bipolar transistor. 1"', 21, 22, 28, 29, and 30 respectively correspond to the aforementioned 1", 19, 20, 25, 26, and 27, forming a second bipolar transistor. 1"' is *n*-type silicon, 23 is p^+-type silicon, 31 is an *n*-type[-material]-side electrode, and 32 is a p^+-type[-material]-side electrode, a p^+n photodiode being formed by 1"', 23, 31, and 32. The first bipolar transistor drives a semiconductor laser, and the second bipolar transistor drives a photodiode. Because this optoelectronic semiconductor device is such that photoreception and photoemission are carried out on a single chip, not only can it be used as a repeater for signal transmission using optical fibers but it can also be applied to use in an optical amplifier, an optical-optical signal converter, or the like. While a p^+n photodiode was used as photodiode in the present working example, a *pin* photodiode or an avalanche photodiode may also be used thereas.

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[8] *Here and below, capital "P" rather than italicized "p" accurately reflects same in Japanese text. —Tr.*

[*Japanese text, sheet 476 (4), Specification, column —13—*]

Working Example 3

Another working example of the present invention is shown in FIG. 3. This working example is characterized by the fact that both the front and the back surface of a silicon substrate are used to constitute an optoelectronic semiconductor device.

At FIG. 3, 33 is a *p*-type[9] monocrystalline silicon substrate, both the front and the back surface of which have been polished to a mirror finish. The substrate has a (100) facial orientation and an impurity concentration on the order of 1×10^{15} cm^{-3}. 34 through 40 and 41 correspond to 2 through 8 and 16 indicated [with reference to] Working Example 1, a laser element being constituted at the back face of the monocrystalline silicon substrate. 35, and 36 through 40, are compound semiconductor thin films grown using the graphoepitaxial method and the ordinary epitaxial method, respectively. 41 and 42 are metal electrodes.

43 is an n^+-type source or drain region for a MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) formed on the back face of the p^--type monocrystalline silicon substrate of 33. This n^+-type region [may be] formed by the ion implantation method or the diffusion method. 44 is a gate insulator film, 45 is a gate electrode, 46 is an insulator film for [*Japanese text, sheet 476 (4), Specification, column —14—*] surface passivation, and 47 is metal wiring traces. A MOSFET formed on the front face constitutes an electronic circuit possessing signal processing and operational [logic] capabilities. Electronic element(s) that drive photoreceptive/photoemissive

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[9] *English translation accurately reflects Japanese text. Allowance for possible typographical error in Japanese text would make this* "p^--type." —*Tr.*

element(s) formed on the back face may be formed on the front or back face[10] of the silicon substrate. Photoreceptive element(s) may also be formed likewise. Because such plurality of elements are organically coupled[11] and are controlled by an electronic circuit possessing operational [logic] capability, [they] may be utilized as an interface for a terminal or a repeater for an optical signal transmission system using optical fibers.

Effects of the Invention

The present invention has effects such as the following.

<1> Integration of a plurality of photoemissive elements/photoreceptive elements, electronic drive elements, and signal processing [and] operational [logic] elements on the same substrate is permitted. Furthermore, integration facilitates device miniaturization, and an optoelectronic semiconductor device having high reliability can be obtained.

<2> Because an SiO_2 or other such inactive insulator layer is formed as an intermediate layer over silicon substrate [prior to formation of] compound semiconductor thin film, contamination of monocrystalline silicon substrate by impurities during [*Japanese text, sheet 477 (5), Specification, column —15—*] compound semiconductor thin film growth can be avoided. Furthermore, there is little mutual interference between electronic element(s) on the silicon substrate surface and element(s) comprising compound semiconductor thin film(s), and electrical controllability of the device is good. Furthermore, device design is also facilitated.

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[10] *There appears to be a typographical error in the Japanese text at this location. —Tr.*

[11] *Depending on context, which is ambiguous here, term in Japanese text may also be translated as* "bonded." — *Tr.*

<3> The problem of lattice defects and lattice strain due to lattice mismatch is no longer present with monocrystal(s) grown as a result of introduction of graphoepitaxial techniques, and elements having good characteristics can be obtained. Furthermore, because many varieties of compound semiconductor monocrystals can be grown, many varieties of optoelectronic semiconductor devices can be constructed.

<4> Because introduction of existing planar silicon techniques to silicon photodiodes and electronic silicon elements formed on the surface of monocrystalline silicon substrate is permitted, fabrication of elements excelling not only in performance and reliability but also in versatility is permitted.

<5> Monocrystalline silicon substrate can be mass-produced and large-area [specimens] can be purchased cheaply. Furthermore, monocrystalline silicon substrate quality is satisfactory. Accordingly, because an optoelectronic semiconductor device employing monocrystalline silicon substrate can be mass-produced with good yield, [it] will be inexpensive.

[*Japanese text, sheet 477 (5), Specification, column —16—*]

4. BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 through FIG. 3 show simplified [depictions] of specific working examples of the present invention. FIG. 1 is a drawing showing a working example in which a semiconductor laser element and a silicon electronic drive element are integrated on the same silicon substrate; FIG. 2 is a drawing showing a working example in which a semiconductor laser element, a silicon photoreceptive element, and an electronic silicon drive element are integrated; and FIG. 3 is a drawing showing a semiconductor laser on a silicon substrate surface, working example(s) in

which drive element(s) and signal processing and operational [logic] element(s) are integrated on the surface being respectively shown[12].

1	*n*-Type monocrystalline silicon substrate
1', 1", 1"'	*n*-Type monocrystalline silicon
2, 2', 34	Amorphous insulator film
3, 3, 35	Monocrystalline gallium arsenide thin film[13]
4, 4', 36	*n*-Type monocrystalline aluminum/gallium/arsenic
5, 5', 37	Monocrystalline aluminum/gallium/arsenic
6, 6', 38	*p*-Type monocrystalline aluminum/gallium/arsenic

[*Japanese text, sheet 477 (5), Specification, column —17—*]

7, 7', 39	*n*-Type gallium/arsenic
8, 8', 40	*p*-Type gallium/arsenic
9	p^+-Type silicon layer
10	n^+-Type silicon layer
11	Surface passivation film
12	Surface protection film
13	Electrode
14	Electrode
15	Wiring traces
16, 16', 41	Electrode
17	*p*-Type monocrystalline silicon substrate

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[12] *Slight awkwardness and ambiguity accurately reflects same in Japanese text. —Tr.*

[13] *There appears to be a typographical error in the Japanese text with regard to the reference numerals at left. Reference numerals here accurately reflect those in Japanese text. —Tr.*

18	p^+-Type diffusion layer
19, 21, 23	p^+-Type diffusion layer
20, 22	n^+-Type diffusion layer
24	Surface passivation film
25 through 32	Metal electrode
33	p^--Type monocrystalline silicon substrate
42	Electrode
43	n^+-Type source/drain region
44	Gate insulator film

[*Japanese text, sheet 477 (5), Specification, column —18—*]

45	Gate electrode
46	Insulator film for surface passivation
47	Metal wiring traces

END

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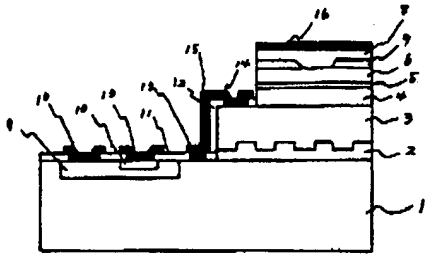
[Seal:]	[*Illeg.*]

[*Japanese text, sheet 478 (6), Drawings*]

FIG. 1



第 1 図

FIG. 2

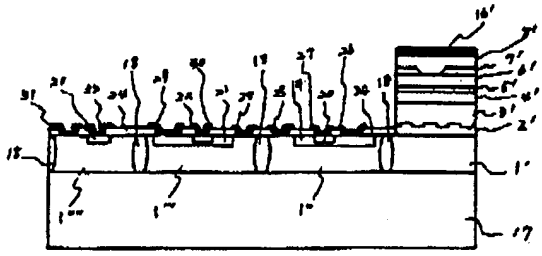
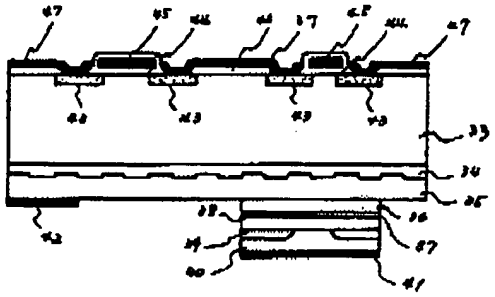


FIG. 3



第 3 図

⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　昭61－108187

⑤Int.Cl.⁴	識別記号	庁内整理番号	㊸公開　昭和61年(1986)5月26日
H 01 S 3/18		7377－5F	
H 01 L 21/203		7739－5F	
27/15		6819－5F	
31/02		7733－5F	審査請求　未請求　発明の数 1　（全6頁）

㊹発明の名称　半導体光電子装置

㉑特　願　昭59－230947
㉒出　願　昭59(1984)11月1日

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㉔代理人　弁理士　最上　務

明　細　書

1　発明の名称

半導体光電子装置

2　特許請求の範囲

(1)　シリコン単結晶基板と、該シリコン単結晶基板の表又は裏面の全体又は一部に存在する非晶質絶縁膜と、該非晶質絶縁膜表面の全体又は一部に存在する化合物半導体薄膜と、該化合物半導体薄膜表面の全体又は一部に存在する多層化合物半導体薄膜から成ることを特徴とする半導体光電子装置。

(2)　前記化合物半導体薄膜は前記非晶質絶縁膜表面へグラフォエピタキシャル成長法により形成した単結晶薄膜より成り、前記多層化合物半導体は前記化合物半導体薄膜表面へエピタキシャル成長法により形成した多層の単結晶薄膜より成ることを特徴とする特許請求の範囲第1項に記載の半導体光電子装置。

(3)　前記シリコン単結晶基板と、前記化合物半導体薄膜と、前記多層化合物半導体薄膜のうち少なくとも一つを、電子・光変換機能を有する発光素子又は光・電子変換機能を有する受光素子の構成材料として用いたことを特徴とする特許請求の範囲第1項に記載の半導体光電子装置。

(4)　前記シリコン単結晶基板の表又は裏面に、シリコン半導体より成る前記発光素子又は前記受光素子を作動せしめる電子素子と、信号の処理および演算の機能を有する複数の電子素子のうち少なくとも一つを形成したことを特徴とする特許請求の範囲第1項又は第3項に記載の半導体光電子装置。

3　発明の詳細な説明

〔産業上の利用分野〕

本発明は半導体光電子装置の基板構造と機能に関する。

〔従来の技術〕

光の高速性、多重性、精密性等の特長を生かし

て、電子技術の代わりに情報伝送や情報処理に光技術が導入され始めている。例えば、光ファイバとレーザ光を利用しての長距離光通信技術や、光ディスクと半導体レーザを組み合わせた音声並びに画像の再生技術などはその代表的な例である。これらの光システムにおいては、レーザ光等を発する発光素子と、伝送光信号を電気信号に変換する受光素子と、それらの発光・受光素子を駆動する電子装置はいわば光システムの心臓部である。システムの小型化、高機能化、高速化などのために、これらの光素子と電子装置が一体化され始めている。すなわち、半導体レーザ(LD)やフォトダイオード(PD)と電界効果トランジスタ(FET)を同一半導体基板表面に作り、LDやPDをFETで駆動している。例えば、昭和59年度電通学会講演論文集4-28、講演番号974のようにりん化インジウム化合物半導体基板上に、インジウム・ガリウム・ひ素・りん系の化合物半導体より成るLDと、りん化インジウムFETを作製し、レーザ光をFETで変調している。また同論文集4

-24、講演番号970のようにフォトダイオードとFETを同一基板表面に作製している。このような半導体光電子装置に用いる半導体基板は従来りん化インジウム(InP)基板やひ化ガリウム(GaAs)基板が主に使われている。これらの基板上には特性の良い半導体レーザ素子を作り易い。

一方、シリコン基板上に化合物半導体を成長させて、半導体光電子装置を作製しているものもある。昭和59年度電通学会講演論文集2-17、講演番号255ではシリコン単結晶基板上にゲルマニウムをエピタキシャル成長させ、さらにその表面にひ化ガリウムをエピタキシャル成長させて、そのひ化ガリウムにFETを作っている。また、*The 16th Conference on Solid State Devices and Materials* 1984、講演番号C11では前述の例と同様にゲルマニウムを介してシリコン単結晶基板上にひ化ガリウムを結晶成長させたのち、その表面にレーザダイオードを作りパルス発振させている。

〔発明が解決しようとする問題点〕

しかし、前述の従来技術は次のような問題点をもつ。すなわち、化合物半導体を基板にしたFETなどの電子素子には駆動電圧を高くできない、MIS(*Metal-Insulator-Semiconductor*)界面に単位が多く閾値電圧を制御しにくい、正孔の移動度が小さい、禁制帯幅が広すぎるといった特性を左右する問題点の他に、安定性・信頼性に乏しいといった問題点がある。また、化合物半導体基板自体にも、結晶性が悪い、基板価格が高い、割れやすい、大口径化が困難といった問題がある。したがって従来の化合物半導体基板を用いた半導体光電子装置には実用に際し十分満足できる特性のものが得られていない。

シリコン単結晶基板を用いたものについては、シリコン単結晶とひ化ガリウム単結晶の格子格数に4%以上の差があるため、それらの結晶間に格子不整合が生じる。そのためひ化ガリウム単結晶に格子歪みや格子欠陥が起き、ひ化ガリウム単結晶上の電子素子や光素子の特性に良いものが得られ

ず、信頼性および再現性に欠けるといった問題点があった。

そこで本発明はこのような問題点を解決するためのもので、その目的とするところは、特性に優れ信頼性の高い発光素子、受光素子および電子素子を同一基板上に集積化して、実用性の高い半導体光電子装置を提供するところにある。

〔問題点を解決するための手段〕

本発明の半導体光電子装置はシリコン単結晶基板と、該シリコン単結晶基板の表又は裏面の全体又は一部に存在する非晶質絶縁膜と、該非晶質絶縁膜表面の全体又は一部に存在する化合物半導体薄膜と該化合物半導体薄膜表面の全体又は一部に存在する多層化合物半導体薄膜から成り、前記化合物半導体薄膜はグラフォエピタキシャル成長法により形成した単結晶薄膜より成り、前記多層化合物半導体薄膜はエピタキシャル成長法により形成した多層の単結晶薄膜より成り、前記シリコン単結晶基板と前記化合物半導体薄膜と、前記多層化合物半導体薄膜を発光素子又は受光素子の構成

材料として用い、前記シリコン単結晶基板の裏又は表面にシリコン半導体より成る発光素子又は受光素子を作動せしめる電子素子と、信号の処理および演算の機能を有する電子回路を形成したことを特徴としている。

〔実施例1〕

第1図に本発明の一実施例を示す。第1図において、1は面方向が(100)で不純物濃度が10^{15} cm^{-3}程度のn形シリコン単結晶基板である。2は前記n形シリコン基板表面に熱酸化法または化学気相成長法あるいはスパッタ法などにより形成した厚さ数ミクロンのSiO_2(二酸化シリコン)より成る非晶質絶縁膜である。この非晶質絶縁膜の表面に深さ10～10000オングストローム程度、幅0.1～10ミクロン程度の矩形のストライプ溝を0.1～10ミクロンピッチにエッチングにより形成する。エッチング法には、フッ化水素系のエッチャントを用いる湿式エッチング法やフレオン(CF_4)等を反応性ガスとして用いる反応性イオンエッチング法などがある。溝の長さ方向は任意で

ある。非晶質絶縁膜として本実施例ではSiO_2を使用したが、その他に窒化シリコン(Si_3N_4)、アルミナ(Al_2O_3)等が使用できる。3は前記非晶質絶縁膜上にグラフォエピタキシャル成長したn形のひ化ガリウム単結晶薄膜である。ひ化ガリウム単結晶のグラフォエピタキシャル成長は、まず気相成長法あるいは有機金属気相成長法あるいは分子線エピタキシャル法などにより、非晶質あるいは多結晶のひ化ガリウム薄膜を2に示すような溝のあるSiO_2膜等の表面に堆積させ、次にレーザ又は赤外線ランプ又はヒーター等を用いて加熱し、ひ化ガリウムを溝に沿って再配列させることで単結晶成長できる。グラフォエピタキシャル成長させたひ化ガリウム単結晶の膜厚は数～数十ミクロンである。ひ化ガリウムの表面上での単結晶性を良くするために、グラフォエピタキシャルひ化ガリウム結晶表面に液相成長法や気相成長法など熱平衡成長法により膜質の良い単結晶ひ化ガリウムを成長させても良い。グラフォエピタキシャル法はひ化ガリウムだけでなく、他のⅢ－Ⅴ族系化合物

半導体、Ⅱ－Ⅵ族系化合物半導体、Ⅳ族化合物半導体、シリコンおよびその他の結晶の成長に活用できる。第1図の4～8は3を含めてダブルヘテロ構造のp－n接合半導体レーザを構成している化合物半導体薄膜である。4はn形のアルミニウム・ガリウム・ひ素単結晶より成る第一クラッド層、5は低不純物濃度のアルミニウム・ガリウム・ひ素単結晶より成る活性層、6はp形のアルミニウム・ガリウム・ひ素単結晶より成る第二クラッド層、7はn形のガリウム・ひ素より成る電流制限層、8はp形のガリウム・ひ素より成る表面キャップ層である。本実施例ではダブルヘテロ構造の半導体レーザダイオードを作製しているが、この他に分布帰還形レーザ、多重量子井戸又は超格子レーザ等の作製も可能である。16は8のp形のガリウム・ひ素層よりオーミックコンタクトをとるためのAu－Zn/Auより成る電極である。

9はn形シリコン単結晶基板内に不純物導入して形成したp^+形層、10は前述のp形層中に不純物導入して形成したn^+形層である。1，9および

10でnpn型バイポーラトランジスタを形成する。すなわち1がコレクタ、9がベース、10がエミッタである。11はシリコン基板の表面パッシベーション膜、12は化合物半導体層の表面保護膜である。13はシリコンからオーミックコンタクトをとるAl電極である。14はn形のひ化ガリウム単結晶薄膜よりオーミックコンタクトをとるAu－Ge/Au電極である。15は配線である。

第1図の構造ではバイポーラトランジスタのコレクタ部に半導体レーザダイオードのn側が接続されている。さらに半導体レーザダイオードのp側を正電位に、バイポーラトランジスタのエミッタを負電位にして、バイポーラトランジスタのベースにある電位を与えることにより、半導体レーザダイオードに電流が流れてレーザ発振し、この半導体光電子装置はレーザ光を出射する。出射するレーザ光の強度はバイポーラトランジスタのベース電流で制御できる。

本実施例は半導体レーザと駆動用バイポーラトランジスタを集積化した半導体光電子装置の一例

である。バイポーラトランジスタの代わりに電界効果トランジスタ、静電誘導トランジスタ等を用いても良い。さらに、複数の半導体レーザ、複数のトランジスタ集積してもかまわない。

〔実施例2〕

第2図に本発明の第2の実施例を示す。本実施例の特徴は、半導体レーザとフォトダイオードと駆動用トランジスタを同一基板表面に集積化したところにある。

第2図中17はp形シリコン単結晶基板である。1'は前記p形シリコン単結晶基板上にエピタキシャル成長したn形シリコン単結晶膜である。本n形シリコン単結晶膜の仕様と使用目的は実施例1に記述した1のn形シリコン単結晶基板と同一である。第2図中2'～8'および16'は実施例1に記述した2～8および16に対応する。18は素子分離用のP^+形拡散層である。19，21，23はP^+形拡散層、20，22はn^+形拡散層である。24はシリコンの表面パッシベーション膜、25～32はシリコンのそれぞれの領域からオーミックコンタ

クトをとる金属電極である。1"がコレクタ、19がベース、20がエミッタであり、25，26，27はそれぞれコレクタ、ベースエミッタの電極であり、第1のバイポーラトランジスタを形成する。1"，21，22，28，29および30は前述の1"，19，20，25，26および27にそれぞれ対応し、第2のバイポーラトランジスタを形成する。1'はn形シリコン、23はp^+形シリコン、31はn形側電極、32はp^+形側電極で、1'，23，31および32でp^+nフォトダイオードを形成している。第1のバイポーラトランジスタが半導体レーザを、駆動し、第2のバイポーラトランジスタがフォトダイオードを駆動する。この半導体光電子装置は1チップで受光と発光が行なえるため、光ファイバによる信号伝送の中継器として使えるばかりでなく光増幅器や光－光信号変換器などに応用できる。フォトダイオードには本実施例ではp^+nフォトダイオードを用いたが、他にpinフォトダイオード、アバランシェフォトダイオードも使用できる。

〔実施例3〕

本発明のもう一つの実施例を第3図に示す。この実施例の特徴はシリコン基板の表裏両面を利用して半導体光電子装置を構成したところにある。

第3図において、33は表裏両面共に研磨鏡面仕上げされたp形シリコン単結晶基板である。基板の面方向は(100)で不純物濃度は$1\times10^{15}\,cm^{-3}$程度である。34～40および41は実施例1に示した2～8および16に対応し、シリコン単結晶基板裏側面でレーザ素子を構成している。35はグラフォエピタキシャル法にて、36～40は一般のエピタキシャル法にてそれぞれ成長させた化合物半導体薄膜である。41および42は金属電極である。

43は33のp^-形シリコン単結晶基板裏側面に形成したMOSFET (*Metal-OXide-Semiconductor Field Effect Transistor*) のn^+形ソース又はドレイン領域である。このn^+形領域はイオン注入法又は拡散法により形成する。44はゲート絶縁膜、45はゲート電極、46は表面パッシベー

ション用絶縁膜、47は金属配線である。表側面に形成されたMOSFETは信号処理および演算機能を有する電子回路を構成している。裏側面に形成されている受光・発光素子を駆動する電子素子をシリコン基板の表又は裏奈面に形成しても良い。受光素子も同様に形成して良い。これらの複数の素子は有機的に結合されており、演算機能を有する電子回路で制御されるため、光ファイバを用いた光信号伝送系の中継器や端末のインターフェイスとして活用できる。

〔発明の効果〕

本発明には次のような効果がある。

① 同一基板上に複数の発光素子、受光素子、駆動用電子素子および信号処理演算素子を集積できる。また、集積化することによって装置の小形化が容易となり、信頼性の高い半導体光電子装置が得られる。

② 化合物半導体薄膜はシリコン基板上へSiO_2等の不活性絶縁膜を中間層として形成されるので化合物半導体薄膜形成時に、シリコン単結晶基板

中への不純物汚染を避けられる。また化合物半導体薄膜より成る素子と、シリコン基板表面上の電子素子とは相互干渉が少なく装置の電気的制御性が良い。また装置の設計がしあい。

③ グラフォエピタキシャル技術の導入により成長させた単結晶の格子不整合による結晶歪みや結晶欠陥の問題がなくなり特性の良い素子が得られる。また多種類の化合物半導体単結晶を成長できるため、多種類の半導体光電子装置が構成できる。

④ シリコン単結晶基板表面に形成するシリコン電子素子やシリコンフォトダイオードには既存のシリコンプレーナ技術が導入できるので、性能や信頼性はもちろん、機能性に優れた素子を作ることができる。

⑤ シリコン単結晶基板は大量生産され、大面積のものが安価に入手できる。またシリコン単結晶基板の質も良好である。したがってシリコン単結晶基板を使った半導体光電子装置は歩留り良く大量生産できるので安価である。

4. 図面の簡単な説明

第1図から第3図に本発明の具体的な実施例の概略を示す。第1図は同一シリコン基板上に半導体レーザ素子と、駆動用シリコン電子素子を集積化した実施例を示す図、第2図は半導体レーザ素子とシリコン受光素子と駆動用シリコン電子素子を集積化した実施例を示す図、そして第3図はシリコン基板表面に半導体レーザーを示す図、そして表面に駆動用素子および、信号処理演算素子を集積化した実施例をそれぞれ示す。

1 … n形シリコン単結晶基板

1′, 1″, 1‴ … n形シリコン単結晶

2, 2′, 34 … 非晶質絶縁膜

3, 3, 35 … ひ化ガリウム単結晶薄膜

4, 4′, 36 … n形アルミニウム・ガリウム・ひ素単結晶

5, 5′, 37 … アルミニウム・ガリウム・ひ素単結晶

6, 6′, 38 … p形アルミニウム・ガリウム・ひ素単結晶

7, 7′, 39 … n形ガリウムひ素

8, 8′, 40 … p形ガリウムひ素

9 … シリコン p^+ 形層

10 … シリコン n^+ 形層

11 … 表面パッシベーション膜

12 … 表面保護膜

13 … 電極

14 … 電極

15 … 配線

16, 16′, 41 … 電極

17 … p形シリコン単結晶基板

18 … p^+ 形拡散層

19, 21, 23 … p^+ 形拡散層

20, 22 … n^+ 形拡散層

24 … 表面パッシベーション膜

25〜32 … 金属電極

33 … p^- 形シリコン単結晶基板

42 … 電極

43 … n^+ 形ソース・ドレイン領域

44 … ゲート絶縁膜

45 … ゲート電極

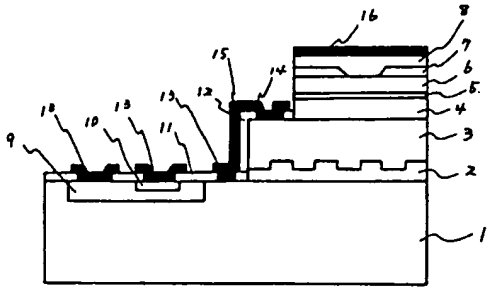
46 … 表面パッシベーション用絶縁膜

47 … 金属配線

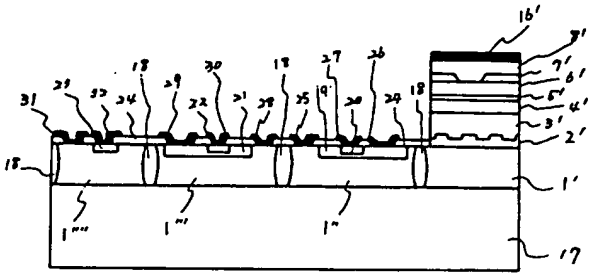
以 上

出願人 株式会社 諏訪精工舎

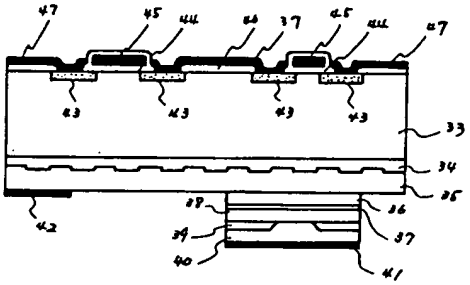
代理人 弁理士 最 上 務



第 1 図



第 2 図



第 3 図